PC03Q
Qbus Time Code Processor

Operation Manual

CHAPTER ONE
INTRODUCTION

1.0 GENERAL

The PCO3Q Qbus Time Code Processor Operation and Technical Manual provides the following information:

- General Introduction and Definition of Terms
- Installation and Setup Details
- Software Interface Details
- I/O Signal Information
- Theory of Operation
- Drawing Set

1.1 PCO3Q FEATURES

The salient features of the PCO3 Time Code Processor include:

- Decodes commonly used time code formats: IRIG A, ITIG B, IRIG G, 2137, XR3, NASA 36.
- Allows zero latency access to decoded time.
- Provides microsecond resolution when decoding in real-time.
- Provides carrier resolution when decoding in non real-time.
- Provides a programmable interval heartbeat interrupt.
- Provides two programmable time coincidence strobes and one interval gate output.
- Allows time capture via an external heartbeat interrupt.
- Operates via Qbus Programmed I/O transfers and supports four interrupt levels using the position independent four-level interrupt scheme.
- VAX/VMS compatible device driver available.
- Local or Remote I/O Panel signal connections available.
- Its 64 byte block of registers can be located on any 64 byte boundary in the Qbus I/O address space.
- Drives optional Bancomm LED display modules with decoded time.

1.2 PCO3Q OVERVIEW

The PCO3Q is a quad height Qbus module designed to decode serial time code signals and provide additional capabilities not normally found on a single board time code reader. The module is designed to operate in DEC MicroPDP-11 and MicroVAX computer systems. It consists of a single quad height printed circuit board and an I/O Panel. The I/O Panel is on a remote "Type B" insert for MicroPDP11 and MicroVAX systems and on a BA200 Series Bulkhead Type H3655 Single Cover for MicroVAX systems.

The operation of the PCO3Q is controlled by registers written and read by the host via Qbus Programmed I/O transfers. There are a total of 29 such software controlled registers. These registers are used for: Defining the time code translation modes of operation; Activating time capture operations; Holding the captured time, input time code error status, and PLL oscillator synchronization status; Defining on-board interrupt priority levels; Enabling the Qbus interrupts; Defining the two coincidence times for generating two time coincidence strobes (which in turn generate an Interval Gate Output); Clearing the Interval Gate Output; and Defining the mode of operation of and programming the time interval of a Heartbeat Interval Counter.

The principal performance characteristics are listed in Table 1-1. The PCO3Q Module is shown in Figure 1-1.

Table 1-1
PCO3Q Performance Specifications

Item	Description
Time Code Reader	
Time Code Formats	IRIG A, B, G, XR3, 2137, NASA 36
Carrier Range	250Hz to 500KHz
Code Direction	forward and reverse
Modulation Ration	3:1 to 6:1
Input Amplitude	500 mV to 10 volts peak-peak
Input Impedance	> 10K Ω
Qbus Interface	
Computer Systems	DEC MicroPDP-11 and MicroVAX supporting the Q-22 bus.
Programmed I/O Base Address	760000_8 - 777776_8 switch selectable address range
	BS7 decoded for A21 - A13. A12 - A6 switch selectable. A5 - A0 select individual registers.
PI/0 Transfer Types	DATI (Data Word Input) DATO (Data Word Output)

Interrupt Levels	4 interrupt levels supported. Position-independent 4-level interrupt scheme.
	Each of the four interrupt sources are software programmable to any of the four Qbus interrupt levels independently
Interrupt Levels	4 interrupt levels supported. Position-dependent 4-levels interrupt scheme.
	Each of the four Interrupt Sources are software programmable to any of the four Qbus interrupt levels independently.
Interrupt Vector	The address of the vector address is software programmable.
DMA	Not used.
Software Compatibility	VAX/VMS with optional PCO3Q I/O device driver.
Electrical Interface	A and B Qbus connectors. Qbus compliant receivers and drivers. One unit load per line.
PCB Mounting	One Qbus slot via A, B, C, D, connectors.
PCB Dimensions	10.457" x 8.43 " quad-height.
I/O Panel	Remote I/O Panel for MicroPDP-11 and MicroVAX on an I/O distribution panel "Type B" insert. Local I/O Panel for MicroVAX on a BA200 Series Bulkhead Type H3655 Single Cover.
Power	+5VDC @ 3.5 A
	+12vdc @ 200 mA
Timing (at the Qbus)	
DATI:	
DIN set to RPLY set	= 125 nsec for all regs except
	= 225 nsec for CTC registers
	= 175 nsec for BIM registers
RPLY set to placing data	= -25 nsec
DIN reset to RPLY reset	= 50 nesec
RPLY reset to remove data	= 10 nsec
Total time contributed to each DATI asynchronous (handshake) transfer by PC03Q	= 185 nsec for all regs. except
	= 285 nsec for CTC registers
	= 235 nsecf for BIM registers

DATO:	
DOUT set to RPLY set	= 125 nsec for all regs. except
	= 225 nsec for CTC registers
	=175 nsec for BIM registers
DOUT reset to RPLY reset	= 50 nsec
Total time contributed to each DATI asynchronous (handshake) transfer by PC03Q	= 175 nsec for all regs except
	= 275 nsec for CTC registers
	= 225 nsec for DBIM registers
PCO3Q Interrupts	
IAK set to BIRQ reset	= 130 nsec
IAK set to RPLY set	= 135 nsec
RPLY set to placing Vector	= -55 nsec
DIN reset to TPLY reset	= 80 nsec
REPLY reset to removing Vector	= 65 nsec
Total time contributed to each interrupt transaction by PC03Q.	= 280 nsec
TTL Input Signals	
Event Trigger	TTL, Positive or Negative Edge Triggered, 50 ns minimum. Width, 1µs minimum period.
TTL Output Signals	
Strobe #1	LSTTL, Active Hi or Lo, 1 clock wide
Strobe #2	LSTTL, Active Hi or Lo, 1 clock wide
Interval Gate	LSTTL, Active Hi or Lo
Interval Counter	LSTTL, Active Lo, 1 clock wide
PDC Signals	LSTTL
Operating and Storage Environment	
Temperature	
Operating	0° to 45° C
Non-operating	-40° to 60° C
Relative Humidity	
Operating	10% to 80% (non-condensing)
Non-operating	5% to 95% (non-condensing)

Altitude	
Operating	1000 ft. Below sea level to 10,000 ft. Above sea level.
Non-operating	1000 ft. Below sea level to 20,000 ft. Above sea level.
Flammability	PCB is UL rated 94V-0

1.3 TIME CODE FORMATS

The widespread use of coded timing signals to assist in the correlation of intercept and test data began in the early 1050's. These signals can be decoded in real time to indicate the current Time of Day (TOD) or recorded along with intercept/test data on magnetic tape recorders for post processing and time correlation.

Hundreds of time code formats were developed - one for each agency involved. During the early 1960's the InterRange Instrumentation Group promoted a series of "standard" time code formats now loosely formats: IRIG A, IRIG B, and IRIG G.

Several other formats still enjoy relatively widespread use within their originating agencies: XR3, 2137, and NASA 36. These codes are also processed by the PC03Q.

More complete details on these and other time code formats is available free of charge, on request from either Bancomm Division or Datum Inc in the form of the "Datum Inc, Handbook of Time Code Formats." Figure 1-2 illustrates a frame of IRIG A, B, or G time code.

1.4 TIME CODE RESOLUTION

BCD encoded time-of-day (TOD) is transmitted once per frame with an amplitude modulated signal. The PC03Q Time Code Processor Module decodes the TOD data, once per frame, and counts the number of carrier cycles from the start of the frame, the "on-time mark." ThePC03Q Also provides a phase-locked loop which converts the time code carrier into a 1MHz clock which can be counted instead of the time code carrier. Or one microsecond (when the PLL clock is used at real-time rates.) Table 1-2 details the time resolution for each time code type when the carrier or 1MHz PLL clock is used.

Table 1-2
Time Code Resolution

Format	Carrier Resolution	PLL Resolution
IRIG A	100µsec	1µsec
IRIG B	1msec	1µsec
IRIG G	10µsec	1µsec
2137	1msec	1µsec
XR3	4msec	Not available
NASA 36	1msec	1µsec

1.5 DEFINITION OF TERMS

1pps - One Pulse Per Second. A 1 carrier cycle wide pulse whose low to high going edge occurs on-time.

Capture - The action of latching the current time and holding this time so that it can be read over the Qbus.

Carrier - The sinusoidal signal which when amplitude modulated becomes a time code signal. For example, IRIG B uses a 1KHz carrier.

Clock - The TTL signal used to clock the minor time (subsecond) counters on the PC03Q module. This signal is either at the carrier rate of the input time code or 1MHz.

Event Trigger - An input to the PC03Q whose positive or negative edge can be used to capture time and/or generate in interrupt.

Forward - Denotes the direction of time code where time increases.

Heartbeat - A signal generated by the PC03Q that repeats every N number of CLOCK counts where N is set by the user.

Interval Gate - A signal generated by the PC03Q that is asserted by Strobe #1 and cleared by Strobe #2.

Latency - The interval between when time is requested and when the time can be read over the bus.

Major Time - Hundreds of days through units of seconds.

Minor Time - Hundreds of nsec through units of μsec.

On-Time - The point in the time code frame where the encoded time is true.

PLL - Phased Locked Loop. On the PC03Q, the time code carrier is used in a PLL circuit to generate a 1MHz clock when the time code is running at real-time rates.

Real -Time Rate - The time code rate at which the time code data change by one second for every one real-time second.

Resolution - The least significant digit that can be read from the PC03Q.

Reverse - Denotes the direction of time code where time decreases.

Strobe - A signal generated by the PC03Q which is active for one clock period and occurs at a specified time.

CHAPTER TWO
INSTALLATION AND SETUP

2.0 GENERAL

The PC03Q Time Code Processor Module is a quad height Qbus board designed to be installed in a standard Qbus enclosure. This section details the steps required to setup and install the module in the Qbus chassis.

2.1 BASE ADDRESS SELECTION

Before installing the module in the Qbus chassis the address select DIP switch (SW1) should be setup. The location of SW1 is shown on Figure 1-1. The PC03Q occupies 64 bytes in the Qbus I/O address page and can be freely located on any 64 byte boundary within the Qbus address range 760000_8 - 777776_8.

The 7 DIP switch positions of SW1 correspond to address bits A12 - A6 as shown in Figure 2-1 and determine the base address for the module. (SW1 position 8 is not used.) The base address is defined as the address selected by the SW1 DIP switch when A5 - A0 are 0.

Figure 2-1
DIP Switch SW1

Address Bit	A12	A11	A10	A9	A8	A7	A6
SW1	7	6	5	4	3	2	1

To select a base address, set each of the 7 DIP switches to the ON (same as CLOSED) or OFF (same as OPEN) position. Setting a DIP switch to the ON position selects a logical 0 for the address bit, and the OFF position selects a logical 1.

2.2 LOCAL I/O PANEL (-BA213I/0) INSTALLATION PROCEDURE

The local I/O Panel (Option -BA213I/O) is a BA200 Series Bulkhead Type H3655 Single Cover and is intended for use with MicroVAX series computer systems.

One the base address has been selected as described above, the PC03Q is ready to be installed in the Qbus chassis. When using the local I/O Panel, install the PC03Q as follows:

- Without the Local I/O Panel cables connected to the PC03Q, insert the PC03Q into the Qbus chassis slot.

- Insert the three cables attached to the Local I/O Panel into the corresponding three receptacles on the front of the PC03Q. These cable are keyed, so there is not danger of misconnection.

- Secure the Local I/O Panel to the Qbus chassis by turning the two quarter-turn fasteners.

2.3 REMOTE I/O PANEL (-BA23I/O) INSTALLATION PROCEDURE

The Remote I/O Panel (Option -BA23I/O) is a " Type B" insert and is intended for use with MicroPDP-11 and MicroVAX computer systems. A "Type B" insert is approximately 2.5" x 3.0" and is attached to the chassis with four screws.

Once the base address has been selected a described above, the PC03Q is ready to be installed in the Qbus chassis. When using the Remote I/O Panel, install the PC03Q as follows:

- Remove an unused "Type B" insert from the computer chassis and retain the screws.

- Insert the three cables attached to the Remote I/O Panel into the corresponding three receptacles on the front of the PC03Q. These cables are keyed, so there is no danger of misconnection.

- With the Remote I/O Panel cables connected to the PC03Q, insert the PC03Q into the Qbus chassis slot.

- Secure the Remote I/O Panel to the Qbus chassis using the four screws obtained when the blank insert was removed ealier.

CHAPTER THREE
SOFTWARE INTERFACE

3.0 GENERAL

The PC03Q occupies 64 bytes in the Qbus I/O address page. Refer to Section 2.1 for details on base address selection. Programmed I/O data transfers between the Qbus and the PC03Q are DATI (Data Word Input) and DATO (Data Word Output). This chapter describes the PC03Q registers and their operation.

3.1 REGISTERS

This section describes the PC03Q registers which control the operation of the module. Section 3.2 details the use of these registers to achieve the desired functions. The register map for the PC03Q is listed in Table 3-1. The first column of this table shows the offset from the base address of each register. The column labeled "R/W" shows whether the register is read-only (R), write-only (W), or read/writable (R/W). The data size is either a Word (D0-D15) or Byte (D0-D7) or undefined (--). The value of each register following Qbus initialization (BINIT L asserted) is shown where "- - " indicates the register contents are undefined. A label for each register is listed as is a brief description of the register's function.

Note: All registers must be accessed with word mode instructions despite the size of the data.

3.1.1 CAPTR AND TIME 0-3 REGISTERS

Accessing the CAPTR register with either a read or write causes the time (Days - Microseconds) to be loaded into a bank of latches which freezes the time at the instant the CAPTR register is accessed. Special circuitry on the PC03Q prohibits the time from being latched while the time is changing. This circuitry is designed so that the user can read the time words immediately after an access to the CAPTR register without having to wait some predetermined amount of time (latency) for the time registers to become valid. This is referred to as zero latency time access.

A bank of four word (16-bit) registers holds the captured time. The time data is stored in a packed BCK format as shown in Table 3-2. The time is maintained in these registers until another CAPTR access takes place. An external event trigger or the programmable interval heartbeat pulse can also be used to capture time in the time registers (see Section 3.2).

Table 3-1
PC03Q Register May

Offset Octal	R/W	Data Size	Reset Value	Label	Description
00	R/W	--	--	CAPTR	Capture Time
02	R	W	--	TIMEO	Time Word 0
04	R	W	--	TIME1	Time Word 1
06	R	W	--	TIME2	Time Word 2
10	R	W	--	TIME3	Time Word 3
12	R/W	--	--	CLRIG	Clear Interval Gate
14	R/W	B	00	CR0	Control Register 0
16	R/W	W	00	CR1	Control Register 1
20	R/W	B	00	INTCR0	INT Control Register 0
22	R/W	B	00	INTCR1	INT Control Register 1
24	R/W	B	00	INTCR2	INT Control Register 2
26	R/W	B	00	INTCR3	INT Control Register 3
30	R/W	B	76	INTV0	INT Vector Register 0
32	R/W	B	76	INTV1	INT Vector Register 1
34	R/W	B	76	INTV2	INT Vector Register 2
36	R/W	B	76	INTV3	INT Vector Register 3
40-46	W	W	--	STR1W0-3	Strobe #1 (4 Registers)
50-56	W	W	--	STR2W0-3	Strobe #2 (4 Registers)
60	W	B	--	CTC0	CTC Counter 0 (Heartbeat)
62	W	B	--	CTC1	CTC Counter 1 (Not Used)
64	W	B	--	CTC2	CTC Counter 2 (Not Used)
66	W	B	--	CTCCR	CTC Control Register
70	R/W	--	--	RELFR	Release Capture Lockout

Table 3-2
Time Data Format
(Packed BCD)

Time Reg	Qbus Data Bits (Packed BCD Format)			
	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
TIME0	status bits	days hunds	days tens	days units
TIME1	hours tens	hours units	minutes tens	minute units
TIME2	seconds tens	seconds units	msec hunds	msec tens
TIME3	msec units	µsec hunds	µsec hunds	µsec unitss

Time Status Bits (D15 - D12)		
BIT	Description	
D15	Not used	(Always = 0)
D14	Low Input Signal	0 = Low
D13	1MHz PLL Lock	0 = Locked
D12	Time Code Error	0 = Error

The TIME0 Status Bits are described below.

D14 (Low Input Signal	Time code input signal is either not present or is too low in amplitude.
D13 (1MHz PLL Lock)	PLL circuit has or has not locked to the input time code signal.
D12 (Time Code Error	Indicates valid or invalid time data in the TIME registers.

3.1.2 CRO AND CR1 CONTROL REGISTERS

The two control registers CR0 and CR1 control most of the functions on the PC03Q. CR0 controls selection of the time code format, time code direction (fwd/rev), clock selection (carrier/PLL), and input channel selection. CR1 controls the time coincidence strobes, external event trigger, heartbeat modes, and enables interrupts. Table 3-3 summarizes the function of the bits in CR0. Table 3-4 summarizes the function of the bits in CR1.

3.1.3 STR1W3-0 AND STR2W3-0 TIME COINCIDENCE STROBE REGISTERS

The time coincidence strobe registers are write only and are used to hold the time of day data (Days - Microseconds) for the 2 strobes. STR1W3-0 and STR2W3-0 are sets of four registers whose data format is identical to the packed BCD format for the TIMES3-0

Table 3-3
CR0 Control Register 0

BIT	Name	Function
0	TC0	TC2-0 Selects time code format
		000 = IRIG B 001 = IRIG A
1	TC1	010 = IRIG G 011 = 2137
		100 = XR3 101 = NASA 36
2	TC2	110 = Not Used 111 = Not Used
3	DIR	Time Code Direction 0 = Forward 1 = Reverse
4	CLOCK	Minor Time (Subsecond) Clock 0 = 1MHz PLL 1 = Carrier
		CHSEL1-0 Selects Input Channel
5	CHSELO	00 = Channel 1
		11 = Channel 2
6	CHSEL1	11 = Channel 3
		11 = Channel 4
7	---	Not Used

registers shown in Table 3-2 except that the status bits are ignored.

The Sense (active low or high) of the 2 strobe outputs is controlled by ST1SENSE and ST2SENSE bits 10 and 11 of CR1. The mode (major/minor only) of the 2 strobes is controlled by ST1MODE and ST2MODE bits 8 and 9 of CR1. The interval gate sense is controlled by IGSENSE bit 12 of CR1.

The 2 strobe outputs are enabled with bits 14 and 15 of CR1. It is recommended that the strobe outputs be disabled when modifying STR1W3-0 and STR2W3-0 to prevent false strobe outputs and spurious strobe interrupts.

3.1.4 CTCO AND CTCCR HEARTBEAT INTERVAL REGISTERS

The heartbeat interval pulse registers CTC0 and CTCCR are contained in and 82C54 Counter-Timer Chip (CTC). CTCCR is the control register for the chip control the mode for each of three 16-bit counters contained on the chip. CTC0 is CTC2 are not used on the PC03Q. The HBSYNC bit 13 of CR1 selects whether the counter is synchronized to the time code's 1pps or is free running (no sync).

Table 3-4
CR1 Control Register 1

Bit	Name	Function
0	FREN	Enable Secondary Capture Source 0 = Disable 1 = Enable
1	EVSENSE	Select Sense of Trigger Input 0 = Lo to Hi 1 = Hi to Lo
2	FRSEL	Select Secondary Capture Source 0 = Ext Event 1 = Heartbeat
3	INTEN0	Interrupt Source 0 Int Enable 0 = Disable 1 = Enable
4	INTEN1	Interrupt Source 1 Int Enable 0 = Disable 1 = Enable
5	INTEN2	Interrupt Source 2 Int Enable 0 = Disable 1 = Enable
6	INTEN3	Interrupt Source 3 Int Enable 0 = Disable 1 = Enable
7	---	Not Used
8	ST1MODE	Strobe #1 Mode 0 = Major/Minor 1 = Minor Only
9	ST2MODE	Strobe #2 Mode 0 = Major/Minor 1 = Minor Only
10	ST1SENSE	Strobe #1 Output Sense 0 = Active High 1 = Active Low
11	ST2SENSE	Strobe #2 Output Sense 0 = Active High 1 = Active Low
12	IGSENSE	Interval Gate Sense 0 = Active High 1 = Active Low
13	HBSYNC	Sync Heartbeat to 1pps 0 = No Sync 1 = Sync to 1pps
14	ST1EN	Strobe #1 Output Enable 0 = Disable 1 = Enable
15	ST2EN	Strobe #2 Output Enable 0 = Disable 1 = Enable

3.1.5 CLRIG AND RELFR REGISTERS

The CLRIG register is used to clear the interval gate output. A read from or write to this register will immediately set the interval gate output to this register will immediately set the interval gate output to its inactive state

The REFER register is used to release the time capture lockout that results when a secondary capture source is activated.

3.1.6 INTERRUPT CONTROL AND VECTOR REGISTERS

The PC03Q supports four independent interrupt sources. The four interrupt sources and their relative priority (when two or more sources are assigned to the same Qbus interrupt level) are listed in Table 3-5. Associated with each interrupt source are two registers; one Interrupt Control Register and one Interrupt Vector Register. Interrupt source 0 (Time Coincidence Strobe #2) is INTCR1 and INTV1; etc. Control Register 1 (CR1) bits 3-6 (INTEN0-3) must be set to a logical 1 to enable each interrupt as well. The Interrupt Control Registers and Vector Registers should be setup before the CR1 INTEN bit is set to a logical 1.

3.1.6.1 INTERRUPT CONTROL REGISTERS

The Interrupt Control Registers govern the operation of the Qbus interrupts. There is one control register for each interrupt source, i.e. INTC0 controls interrupt source 0, INTCR1 controls interrupt source 1, etc. The Interrupt Control Register format is shown below. For the Interrupt Control Register, !bus Data Bit 0 and Bits 9-15 are ignored during writes and meaningless for reads.

Qbus	8	7	6	5	4	3	2	1
Function	FLAG	FAC	X/IN	IRE5	IRAC	L2	L1	L0

L2, L1, L0 - Interrupt Level
The 3 interrupt level bits determine the level at which an interrupt will be generated.

L2	L1	L0	INTERRUPT LEVEL
0	0	0	DISABLED
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

IRAC - Interrupt Auto Clear
If the IRAC is set, ITE (Bit 5) is cleared during an interrupt acknowledge cycle responding to this request. This action of clearing IRE disables the interrupt request. To re-enable the interrupt associated with this register, IRE must be set again by writing to the control register, IRE must be set again by writing to the control register.

IRE - Interrupt Enable
This bit must be set to 1 to enable the bus interrupt request associated with the control register.

X/in - External/Internal Vector
This bit must be cleared to 0 in all cases.

FAC - Flag Auto Clear
If FAC is set to 1, the FLAG bit is automatically cleared during an interrupt acknowledge cycle.

FLAG - Flag Bit
Three FLAG bit has not affect on the operation of the interrupts.

Table 3
PC03Q Interrupt Sources

INT	Function
3	External Event Trigger (highest priority)
2	Programmable Heartbeat Pulse
1	Time Coincidence Strobe #1
0	Time Coincidence Strobe #2 (lowest priority)

3.1.6.2 INTERRUPT VECTOR REGISTERS

Each of the four interrupt sources has associated with it an Interrupt Vector Register. Interrupt source 0 uses INTV0, interrupt source 1 uses INTV1, etc. Qbus data bits 1-8 correspond to the Interrupt Vector Register data bits 1-8. Qbus Data Bit 0 and Bits 9-15 are meaningless when reading and writing the Vector Registers.

3.2 FUNCTIONAL DESCRIPTION

Section 3-1 provided and overview of the PC03Q registers and their function. This section provides a description of how these registers are used to achieve the desired functions.

3.2.1 CATURING AND READING TIME

As described in Section 3.1.1, and access to the CAPTR register will freeze the current time, and this time will remain in the TIME3-0 registers until another capture takes place. Two other signals can also be setup to capture time. One source is the External Event Trigger Input. The event input triggers the time capture on either it's low to high to low edge as deterined by the EVSENSE bit (CR1 bit 1). The

other source of time capture is the programmable interval heartbeat pulse. Only one auxiliary source. (i.e. Event or Heartbeat) can be used for time capture at any given instant.

The CAPTR register remains active while a secondary capture source is enabled. The FRSEL bit (CR1 bit 2) selects the secondary capture source, and the FREN bit (CR1 bit 0) enables the secondary capture source to capture time.

Note: The secondary capture sources can always generate an interrupt even if the FREN bit is 0).

When a secondary capture source freezes the time, the TIME3-0 registers will remain frozen until the RELFR register is accessed. That is, all capture sources (including the CAPTR register) will be locked out from capturing a new time. This precludes a capture source from overwriting the time registers before the user program has a change to read them.

3.2.2 EXTERNAL EVENT TRIGGER

The External Event Trigger input provides a means of capturing time based on an event that occurs externally to the PC03Q module. The EVSENSE bit (CR1 bit 1) controls which edge of this input is active. The FREN bit (CR1 bit 0 enables the secondary capture source when set to 1, and the FRSEL bit (CR1 bit 2) selects the External Event Trigger as the secondary capture source when cleared to 0. This input can also generate an interrupt (interrupt source 3) even if it is not enabled to capture time. The Event Trigger input is available on the I/O connectors.

The programmable interval heartbeat pulse can be used to generate a Qbus interrupt and/or capture time. This active low heartbeat pulse is available on the I/O connectors. The heartbeat generator uses a 16-bit counter which counts either the time code carrier or 1MHz PLL clock as determined by the CLOCK bit (CR0 bit 4). The CLOCK bit also determines the time resolution (See Section 3.2.6). The heartbeat pulse can be configured to be synchronized to the time code 1pps or can free run as determined by the HBSYNC bit (CR1 bit 13).

Table 3-6
CTCCR Control Byte

SYNC Mode	CTCCR	Interval
SYNC to 1pps (HBSYNC = 1	072 (Octal)	N+1
FREE RUNNING (HBSYNC = 0)	064 (Octal)	N

A control byte must be written to the CTCCR register before the two byte count is written to the CTCO register. The value of the CTCCR control byte depends on whether the heartbeat is synchronized to the time code 1pps or is free running. Table 3-6 lists the CTCCR control byte values used for both cases. This table also lists the heartbeat interval (number of clock cycles per pulse) for both cases.

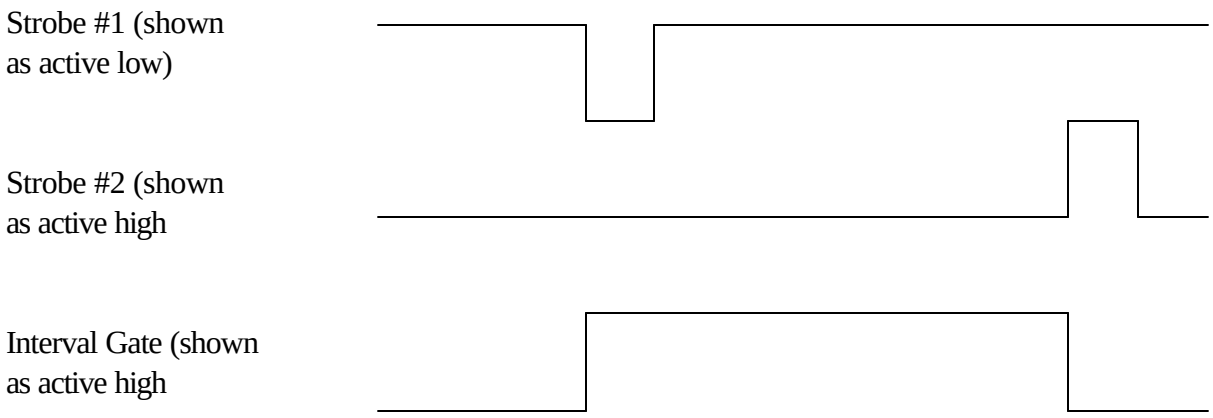
The 16-bit count (N) is written to CTC0 as two consecutive bytes (D0-D7); least significant byte (LSB) first followed by the most repeat every N+1 counts when synchronized to the 1pps; when the counts. (N = the count written into the CTC0 REGISTER.)

As described in Section 3.2.1 the heartbeat pulse can be used to capture time. The FREN bit (CR1 bit 0) enables the secondary capture source when set to 1, and the FRSEL bit (Cr1 bit 2) selects the Heartbeat Interval Pulse as the secondary capture source when interrupt (interrupt source 1.) The heartbeat pulse can also be bused to generate an interrupt (interrupt source 2.) The heartbeat pulse can generate and interrupt even if it is not enabled to capture time.

3.2.3 TIME COINDIDENCE STROBES

Two time coincidence strobes, each of which produces a strobe 1 clock period wide, are provided. Each strobe can be used to generate and interrupt. Strobe #1 is interrupt source 1, and Strobe #2 is interrupt source 0. Each strobe is setup by loading 4 strobe registers (STR1W3-0 or STR2W3-0) with the time of day at which the strobe is to be activated. The format of the strobe data is the same as that shown in Table 3-2 except the status bits are ignored. STR1W0 corresponds to the TIME0 format, etc. The ST1SENSE and ST2SENSE bits (cr1 bits 10 and 11) determine the active sense of must be written into the registers. If the minor time clock source be set to 0. For example, if IRIG B time code is used and the CLOCK bit is set to 1 (carrier) then the three microsecond digits must be set to 0.

Figure 3-1
Strobes and Interval Gate Timing



Note: Interval Gate transition occurs <20 nsec after the strobe is activated.

Two modes of operation (major/minor only) are implemented for each of the strobes. The ST1MODE and ST2MODE bits (CR1 bits 8 and 9) control the mode of operation for strobe #1 and strobe #2. The "major/minor time" mode uses all time digits (days hundreds - microseconds units) for time coincidence comparisons whereas the "minor time only" mode used only subsecond digits (milliseconds hundreds - microseconds units) for time coincidence comparisons. When using the "minor time only" mode ignores the days hundreds - seconds units digits.

The Interval Gate signal is asserted when Strobe #1 is activated and is cleared when Strobe #2 is activated. The sense of the Interval Gate is controlled by the IGSENSE bit (CR1 bit 12). The Interval Gate is cleared by Qbus initialization, but can also be cleared by an access to the CLRIG register. Figure 3-1 shows the timing relationship between the two strobes and the interval gate. The two strobe pulses and the interval gate signals are available on the I/O connectors.

3.2.4 Qbus INTERRUPTS

As described above, there are four sources of Qbus interrupts each of which functions independently. Each interrupt source can be configured to use any of the four (BIRQ4-BIRQ7) Qbus interrupt levels or all four sources can use the same level if desired. Each source enable bits in control register 1 (CR1) must be set to 1 to enable each interrupt source. These enable bits should be 0 until all other control registers (CR0, CR2, INTCRX, INTVX, etc) are setup.

3.2.5 READING TIME AT DIFFERENT RESOLUTIONS

Table 1-2 shows the resolution of each time code format when the carrier is used to clock the minor time counters (CLOCK bit = 1). All less significant digits will be forced to 0 when using the carrier. For example, when reading IRIG B with the carrier clock, the 3 microsecond digits will always be read as 0. XR3 is a special case because its carrier frequency is only 250 Hz. The subsecond digits for XR3 will range from .000 to .249 each second. The XR3 subsecond digits must therefore be multiplied by four to produce the actual subseond count. For example, when a subsecond value of .123 is read, the actual subsecond value is .492 (.492 = 4 .123).

When using the PLL clock (CLOCK bit = 0) the time resolution will be 1 microsecond for all codes except XR3 which will not function with the PLL clock. The PLL clock can be used only at real-time rates. Using the PLL clock at non-real time rates will result in erroneous subsecond counts being read.

3.2.6 READING TIME IN REVERSE

When reading time that has been recorded on a magnetic tape recorder, it is possible to read the time in reverse (i.e. time decreased). The subsecond counters, however, always count up. This means that the subsecond count read in reverse will be increasing instead of decreasing (the major time does decrease). For example, the value of the subsecond count following the on-time mark should be .999999, then .999998, etc., but will be read as .000000, .000001, etc. The minor time count must be converted by subtracting the count read from .999999.

Actual Minor Time =.0999999 - Minor Time Read.

CHAPTER FOUR
I/O CONNECTORS

4.0 GENERAL

Signal I/O on the PC03Q is accomplished via an I/O panel. Two variations of panel design are used by the PC03Q: a remote I/O Panel (Option - BA21I/O) for MicroPDP-11 and MicroVAX systems and a local I/O Panel is on an I/O Distribution Panel "Type B" insert which is located at the rear of a Qbus system cabinet. The local I/O Panel is on a BA200 Series Bulkhead Type H3655 Single Cover which is screwed on to the card enclosure covering over the foreplane edge of the Qbus board. The foreplane edge of the PC03Q contains three flat cable receptacles which mate with cables from the I/O panel (See Figure 1-1.)

Each I/O panel includes four connectors: One BNC for External Event Trigger input; one twenty- five pin D connector socket; and one twenty pin rectangular connector. The location of all connectors on the local and remote I/O panel is shown in Figure 4-1.

4.1 PC03Q CABLE RECEPTACLES

The three flat cable receptacles located on the foreplane edge of the PC03Q mate with the cables from the local and remote I/O panels. This section provides the pin assignments for these connectors for those users who choose to build their own cables and I/O panels.

4.1.1. J1 PDC CONNECTOR

The twenty pin receptacle J1 carriers the PDC signals (described in Section 4.3) which are normally used to drive Bancomm's optional LED display modules. The pinouts for this connector are shown in Table 4-1.

4.1.2. J2 I/O CONNECTOR

The twenty six pin receptacle J2 carriers all PC03Q I/O signals (except for the PDC signals). The pinouts for this connector are shown in Table 4-2.

4.1.3 J5 CHANNEL 1 TIME CODE INPUT AND EXTERNAL EVENT INPUT

The ten pin receptacle J5 carries the Channel 1 Time Code Input and the External Event Trigger Input signals. These signals are connected in parallel with the J2 I/O connector pins which also carry these two signals. The pinouts for this connector are shown in Table 4-3.

Table 4-1
PDC Connector Pinouts (I/O Panel and J1)

J1	Signal Description
1	Ground
2	PDC Enable*
3	D0
4	D1
5	D2
6	D3
7	D4
8	D5
9	D6
10	D7
11	Each Cycle
12	High Cycle*
13	1pps
14-16	Not Used
17	FSYNC*
18	Ground
19	+5 VDC
20	+5 VDC

Table 4-2
PC03Q Pinouts For J2

J2	Signal Description
25	Time Code Channel 1 Input
23	Time Code Channel 2 Input
21	Time Code Channel 3 input
19	Time Code Channel 4 input
17	External Event Trigger Input
15	Heartbeat Pulse Output
13	Interval Gage Output
11	Time Coincidence Strobe #2 Output
9	Time Coincidence Strobe #1 Output
7	1 Pulse Per Second (1pps) Output
8-24 Even	Ground (even numbered pins only)

Table 4-3
J5 Connector Pinouts

J5	Signal Description
2	Time Code Channel 1 Input
9	External Event Trigger Input
1	Ground
3-8	Ground
10	Ground

Table 4-4
25 Pin DS I/O Connector Pinouts (I/O Panels Only)

25 DS	Signal Description
13	Time Code Channel 1 Input
12	Time Code Channel 2 Input
11	Time Code Channel 3 Input
10	Time Code Channel 4 Input
9	External Event Trigger Input
8	Heartbeat Pulse Output
7	Interval Gate Output
6	Time Coincidence Strobe #2 Output
5	Time Coincidence Strobe #1 Output
4	1 Pulse Per Second (1pps) Output
17-25	Ground

4.2 LOCAL AND REMOTE I/O PANEL CONNECTORS

Both the Local I/O Panel and the Remote I/O Panel contain the same set of connectors. This section lists the pin assignments for these connectors. The location of all connectors on the local and remote I/O panels i shown in Figure 4-1.

4.2.1 CHANNEL 1 TIME CODE INPUT BNC

The Channel 1 time code input is available on and I/o Panel BNC and is connected in parallel with the 25 pin DS connector which also carries this signal.

4.2.2 EVENT TRIGGER INPUT BNC

The Event Trigger Input is available on an I/O panel BNC and is connected in parallel with the 25 pin DS connector which also carries this signal.

4.2.3 25 PIN DS SIGNAL I/O CONNECTOR

All I/O signals (except the PDC signal (except the PDC signals) are connected to the I/O panel 25 pin DS connector. The pin assignments for this connector are shown in Table 4-4.

4.2.4 PIN PDC CONNECTOR

The twenty pin rectangular connector carries the PDC (Peripheral Data Connector) signals which can be used to drive the Bancomm LED time display modules. The pin assignments for the PDC connector are shown in Table 4-1.

Table 4-5
PDC Data Format

D7	D6	D5	D4	D3 - D0 (BCD)
0	0	0	0	Days Hundreds
0	0	0	1	Days Tens
0	0	1	0	Days Units
0	0	1	1	Hours Tens
0	1	0	0	Hours Units
0	1	0	1	Minutes Tens
0	1	1	0	Minutes Units
0	1	1	1	Seconds Tens
1	0	0	0	Seconds Units

4.3 PDC SIGNAL DESCRIPTION

The signals carried on the PDC (Peripheral Data Connector) are generally used to drive other Bancomm products which required decoded time such as the PC26XT LED display module. These signals can, however, be used by the user for a variety of applications. Decoded time is transmitted over the PDC once per second using the PDC ENABLE* and D0-D7 lines in a byte serial fashion (i.e. a burst of 9 bytes are sent) just after the 1pps mark. The D0-D7 encoding is shown in Table 4-5. The lower nibble contains the BCD encoded time digit and the upper nibble determines which digit has been transmitted. The D0-D7 data lines are valid when PDC ENABLE* is low. EACH CYCLE is a TTL representation of the time code carrier (high during positive half cycles, low during negative half cycles). HIGH CYCLE* is TTL signal that is low during a portion of a positive high amplitude cycle. 1pps is a TTL signal, one carrier cycle wide, whose rising edge occurs on-time. FSYNC* is a TTL signal, one carrier cycle wide, whose falling edge occurs one per frame at the on-time mark.

CHAPTER FIVE
THEORY OF OPERATION

5.0 GENERAL

This section describes the theory of operation for the PC03Q Module.

5.1 TIME CODE READER

The heart of the PC03Q Module is the circuitry used to convert the serial modulated time code signal into the parallel BCD format which can be read over the Qbus.

One of four channels of time code is selected for decoding through an analog switch. The output of this switch is passed to an automatic gain control (AGC) CIRCUIT TO EQUALIZE THE LEVEL OF THE SIGNAL. The equalized signal drives two slicers; one slicer generates a TTL level "each cycle" clock (high for the positive half of the cycle and low for the negative half or the cycle); the other slicer generates a TTL level "high cycle: signal which is for a portion of the positive high amplitude cycle. These two signals drive the digital time code reader circuity which consists of two PLD's, and EPROM, and a Z8 microcontroller.

The Z8 performs validation of the incoming decoded major time and writes this time to a bank of latches on the surface mount daughter module and to the PDC connector.

5.2 TIME CAPTURE AND MINOR TIME COUNTERS

The minor time (subsconds) is generated by six decade counters which count either carrier cycles or the 1MHz PLL clock. These counters are synchronized to the time code 1pps by a signal generated by the time code decoder. When the counters roll-over to 0, the major time is clocked into a second set of latches.

When a time capture source is activated, all time of day digits (days-microseconds) are clocked into a set of latches which can be read over the Qbus. Special circuitry is employed to assure that the time is not latched during a counter transition. If the time capture coincides with a counter transition then the time capture is held off until the counter outputs settled.

5.3 HEARTBEAT AND STROBES

The programmable interval heartbeat pulse is generated by the 82C54 CTC which is driven by the carrier or 1MHz PLL clock. This counter can be synchronized to the 1pps through it's GATE input.

The time coincidence strobes are generated by a bank of comparators which compares the decoded time to the time strobe in the strobe registers (STR1W3-0 and STR2W3-0). The interval gate is generated by a flip-flop which is set when strobe #1 is activated and reset when strobe #2 is activated.

5.4 QBUS INTERFACE

The Qbus interface consists of the usual assortment of bus transceivers, buffers, and decoders commonly found on any microprocessor based system. 8641 transceivers are used for the data and address bus. 8837 receivers are used for reception of bus control signals. Qbus interrupts are supported with an MC68153 Bus Interrupter Module from Motorola. A +12V DC-DC converter supplies the analog circuitry with -12VDC.

CHAPTER SIX
PROGRAMMING EXAMPLES

6.0 GENERAL

This section provides programming example to illustrate the use of the PC03Q. Examples are shown in a simple pseudo-code. The following two functions are used to indicate Qbus DATI reads from and DATO writes to the PC03Q registers.

```
Read (Reg)              /* Returns data at address offset Reg   */
Write (Data, Reg)       /* Writes data to address offset Reg    */
```

Note: All constants are in base octal**.**

6.1 CAPTURING AND READING TIME

This example shows how to capture time using the CAPTR register then reads the time into the array "TimeArray." The PC03Q is configured for IRIG B, forward, microsecond resolution, channel 1.

```
Write (0,CRO);                  /* Configure CR0 for IRIG B          */
                                /* Forward, PLL clock, ch 1          */
Write (0, CR1);                 /* Disable Ints, disable         */
                                /* Secondary capture source          */
Dummy = Read (CAPTR);           /* Capture time                  */
TimeArray [0] = Read (TIME0);   /* Read 4 time registers             */
TimeArray [1] = Read (TIME1);
TimeArray [2] = Read (TIME2);
TimeArray [3] = Read (TIME3);
```

6.2 EXTERNAL EVENT TRIGGER

This example shows how to setup the control registers and interrupt registers to use the Event Trigger to capture time and generated an interrupt.

```
Write (0,CRO);                  /* Configure CR0 as above            */
Write (0, CR1);                 /* Disable Ints, enable ext          */
                                /* Event for time capture            */
Write (50, INTCR3);             /* Enable Int on level 4         */
Write (Vector, INTV3);          /* Set interrupt vector data         */
Write (101, CR1);               /* Enable Int Source 3               */
Dummy = Read (RELFT);           /* Release Capture Lockout           */
```

```
/* Wait for Interrupt                /*
/* Interrupt Service Routine         /*

TimeArray [0]: = Read (TIME0); etc.
Dummy = Read (RELFR);                /* Release Capture Lockout
```

6.3 TIME COINCIDENCE STROBES

This example illustrates the use of the two strobes and the interval gate without using the interrupts.

```
Write (0,CRO);                       /* Configure CR0 as above          */
Write (6000, CR1);                   /* Strobes are active low,         */
                                     /* Interval gate is active high    */
                                     /* Interrupts are disable          */
                                     /* Strobe Outputs are disabled     */
Write (Strobe1 [0), STR1W0);         /* Enable Int Source 3             */
Write (Strobe1 [1), STR1W1);         /* Release Capture Lockout         */
Write (Strobe1 [2), STR1W2);
Write (Strobe1 [3), STR1W3);


/* Write Strove #2 data          */

Dummy = Read (CLRIG);                /* Clear Interval Gate             */
Write (146000, CR1);                 /* Strobe Outputs are enabled      */
```

6.4 PROGRAMMABLE INTERVAL HEARTBEAT

The first example shows how to use the heartbeat and synchronize it to the 1pps. The heartbeat will repeat every 100 microseconds and is enabled to capture time. When synchronized to the 1pps, the heartbeat repeats every N + 1 (99 + 1) counts.

```
Write (0, CR0);                      /* Configure CR0 as above          */
Write (20005, CR1);                  /* Sync Heartbeat, enable capture  */
Write (72, CTCCR);                   /* CTCCR set for sync option       */
Write (143, CTC0);                   /* CTC count least significant byte */
Write (0, CTC0);                     /* CTC count most significant byte */
```

This example show how to use the heartbeat without 1pps synchronization. The heartbeat will repeat every 380 microseconds and is enabled to capture time and generate and interrupt. Using this mode, the heartbeat repeats every N (380) counts.

```
Write (0, CR0);              /* Configure CR0 as above                    */
Write (5, CR1);              /* No sync, enable capture, disable int      */
Write (52, INTCR2);                /* Enable Qbus Int on level 5          */
Write (Vector, INTV2);             /* Set interrupt vector data           */
Write (64, CTCCR);                 /* CTCCR set for free running option   */
Write (174, CTC0);                 /* CTC Count LSB                       */
Write 1, CTC0);                    /* CTC count MSB                       */
Write (45, CR1);                   /* Enable interrupt source 2           */
```